

Description

[METHOD OF RELIEVING WAFER STRESS]

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The present invention relates to a semiconductor fabrication process. More particularly, the present invention relates to a method of relieving wafer stress.

[0003] Description of the Related Art

[0004] At present, most semiconductor devices are fabricated on silicon wafers. To increase productivity and lower production cost, the diameter of wafers has been increased steadily from 4, 5, 6, 8 inches to 12 inches so that more chips can be fabricated from a single wafer.

[0005] In most semiconductor fabrication processes, a continuous film layer first deposited over a wafer before performing a photolithographic and etching process to pattern the film. For example, in the process of fabricating metallic interconnects, a dielectric layer is formed over a wafer and then patterned to form a via opening or a trench before

depositing metallic material into the via opening or the trench. When the deposited film induces stress in the wafer due to some processing factors (such as a chemical-mechanical polishing operation), the entire wafer may warp. If such wafer stress is not relieved in time, subsequently processing operations is likely to be affected.

[0006] Figs. 1A through 1C are schematic cross-sectional views showing the steps for fabricating conventional metallic interconnects. First, as shown in Fig. 1A, a wafer 100 having a dielectric layer 102 with a plurality of contacts/vias 104 therein is provided. A dielectric layer 106 is formed over the entire wafer 100 to cover the dielectric layer 102 and the contacts/vias 104. Because the dielectric layer 106 may accumulate some internal stress, the wafer 100 is slightly warped.

[0007] As shown in Fig. 1B, a photolithographic process is carried out to form a patterned photoresist layer 108 over the dielectric layer 106. The patterned photoresist layer 108 exposes a portion of dielectric layer 106 where trenches are required. In other words, the photoresist layer 108 exposes the locations for forming the desired metallic lines.

[0008] As shown in Fig. 1C, the exposed dielectric layer 106 is

etched to form a plurality of openings 110. Because the dielectric layer 106 is no longer a continuous sheet after removing a portion of the dielectric layer 106 to form the openings 110, internal stress is relieved so that the wafer returns to its former warp-free state.

[0009] In the aforementioned process, the patterned photoresist layer 108 is formed over a warped dielectric layer 106. Because the wafer 100 will return to its warp-free state as soon as the opening 110 is formed in the dielectric layer 106, the openings 110 may shift relative to the intended positions. As a result, misalignment of the contacts/vias 104 occurs quite frequently.

[0010] Furthermore, the misalignment problem aggravates from the warping center towards the edge of a wafer. Hence, the misalignment problem is particularly serious for a wafer with a larger diameter. For a chips lying in the peripheral region of a wafer, the situation may be so serious that the metallic interconnect process fails to link up a metallic line with a corresponding contact or via. When this happens, performance of the device will deteriorate and yield of the chip will drop.

SUMMARY OF INVENTION

[0011] Accordingly, at least one objective of the present inven-

tion is to provide a stress relieving method for a wafer capable of relieving internal stress within a highly stressed film layer above the wafer.

[0012] At least a second objective of this invention is to provide a stress relieving method for a wafer capable of preventing any misalignment after a photolithographic process due to a warping of the wafer.

[0013] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a stress relieving method for a wafer. A wafer is provided, wherein at least a dielectric layer has already formed over the wafer and the wafer having a first and a second area. At least no circuits are formed on the dielectric layer within the first area. Thereafter, openings are formed in the dielectric layer within the first area. A material layer is formed over the dielectric layer, wherein the material layer is fabricated from a dielectric material or a metal material. Thus, pits are formed on the surface of the material layer at locations above the first opening. Through the pits on the material layer, stress within the material layer is relieved and hence the amount of stress conferred to the wafer is reduced.

[0014] This invention also provides an alternative stress relieving method for a wafer. A wafer is provided, wherein at least a dielectric layer has already formed over the wafer and the wafer having a first area and a second area. At least no circuits are formed on the dielectric layer within the first area. Thereafter, a material layer is formed over the dielectric layer, wherein the material layer is fabricated from a dielectric material or a metal material. A plurality of openings is formed in the material layer within the first area. These openings absorb stress within the material layer so that the amount of stress conferred to the wafer is reduced.

[0015] Accordingly, by breaking up the high stress film layer (the material layer) into a sheet with discontinuous surface and height difference, this invention relieves the stress within the film layer and prevents the warping of the wafer. Therefore, misalignment of photoresist pattern after a photolithographic process is avoided. Furthermore, no additional photomask is required and hence there is no added complexity to the fabrication process.

[0016] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of

the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0017] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0018] Figs. 1A through 1C are schematic cross-sectional views showing the steps for fabricating conventional metallic interconnects.

[0019] Figs. 2A through 2C are schematic cross-sectional views showing the steps for relieving the stress within a wafer according to a first preferred embodiment of this invention.

[0020] Figs. 3A through 3D are schematic cross-sectional views showing the steps for relieving the stress within a wafer according to a second preferred embodiment of this invention.

DETAILED DESCRIPTION

[0021] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which

are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0022] Figs. 2A through 2C are schematic cross-sectional views showing the steps for relieving the stress within a wafer according to a first preferred embodiment of this invention. The stress relieving method can be applied to a metallic interconnect fabrication process. To simplify description and prevent the incorporation of any unnecessary restrictions to this invention, some structure components and their description are omitted below.

[0023] As shown in Fig. 2A, at least a dielectric layer 208 is formed on a wafer 200. Wherein the dielectric layer 208 is a silicon oxide layer, a silicon nitride layer or other common dielectric material layer, for example. According to the type of material chosen, the dielectric layer 208 is formed in a chemical vapor deposition process or a spin-coating process, for example. In addition, the wafer 200 has an area 202 and another area 204. The area 202 is, for example, a die area with semiconductor devices (not shown) thereon. At least no circuits are formed on the dielectric layer 208 with area 204, and the area 204 is the

scribe line on the wafer, for example.

[0024] As shown in Fig. 2B, a plurality of openings 210 are formed in the dielectric layer 208 within the area 202. In the meantime, a plurality of openings 212 is also formed in the dielectric layer 208 within the area 204. The openings 210 and 212 are formed, for example, by performing photolithographic and etching processes. Thereafter, material is deposited into the openings 210 to form a material layers 214. The material layers 214 are fabricated using metallic or other conductive substances. In the metallic interconnect fabrication process, the material layers 214 serves as via plugs. Hence, the material layers 214 are preferably fabricated from tungsten or copper.

[0025] As shown in Fig. 2C, a material layer 216 is formed over the dielectric layer 208, wherein the material layer is fabricated from a dielectric material or a metal material, for example. Due to the processing conditions, the material layer 216 may retain strong residual stress. Because the openings 212 within the area 204 has no material fillings, pits 218 are formed on the material layer 216 at locations above the openings 212 so that the material layer 216 has an irregular upper surface.

[0026] The aforementioned stress relieving method for wafer in-

cludes forming a plurality of openings 212 in the area 204 without any circuits so that a material layer 216 deposited over the wafer contains pits 218. Hence, the material layer 216 no longer forms a continuous smooth surface.

Through the pits 218, internal stress within the material layer 216 is relieved so that the wafer is prevented from warping. As a result, misalignment of the patterns formed by a subsequent photolithographic and etching processes due to warping can be avoided.

[0027] Furthermore, the openings 212 for relieving stress and the openings 210 for fabricating semiconductor devices may be formed in a single photolithographic/etching process. Therefore, the same number of masks as in a conventional process is used. In other words, this invention can be implemented to relieve stress within a film layer and prevent the wafer from warping without adding any complexity to the fabricating process.

[0028] In another embodiment of this invention, different steps are carried out to foster the same stress relieving function. Similarly, to simplify description and prevent the incorporation of any unnecessary restrictions to this invention, some structure components and their description are omitted below. Furthermore, any elements identical to the

first embodiment are labeled identically.

[0029] Figs. 3A through 3D are schematic cross-sectional views showing the steps for relieving the stress within a wafer according to a second preferred embodiment of this invention. As shown in Fig. 3A, at least a dielectric layer 208 is formed on a wafer 200 and the wafer 200 has an area 202 and another area 204. The area 202 is, for example, a die area with semiconductor devices (not shown) thereon. At least no circuits are formed on the dielectric layer 208 with the area 204, and the area 204 is scribe line on the wafer, for example.

[0030] As shown in Fig. 3B, a plurality of openings 210 is formed in the dielectric layer 208 within the area 202. Thereafter, material is deposited into the openings 210a to form material layers 214. The material layers 214 are fabricated using metallic or other conductive substances. In the metallic interconnect fabrication process, the material layers 214 serves as via plugs. Hence, the material layers 214 are preferably fabricated from tungsten or copper.

[0031] As shown in Fig. 3C, a material layer 216 is formed over the dielectric layer 208 covering the entire wafer 200, wherein the material layer 216 is fabricated from a dielectric material or a metal material, for example. As shown in

Fig. 3D, a plurality of openings 218a are formed in the material layer 216 within the area 204 so that the smooth material layer 216 is patterned. The openings 218a are formed, for example, by performing photolithographic and etching processes.

[0032] The second embodiment of this invention uses a series of steps that differs from the first embodiment. However, they both use the same idea of breaking up the continuous material layer 216 to reduce stress within the material layer 216. With the internal stress within the material layer 216 removed, the wafer is prevented from warping. As a result, misalignment of the patterns formed by a subsequent photolithographic and etching processes due to warping is similarly avoided.

[0033] In the first embodiment, each opening 212 exposes a film layer (the wafer 200 in Fig. 2B) underneath the dielectric layer 208 and provides a through hole. However, the opening 212 may not reach too deep to expose the film layer underneath the dielectric layer 208 so that only a groove is formed. Similarly, the openings 218a in the second embodiment can be through holes or grooves.

[0034] Although a metallic interconnect fabrication process is used as an example in both embodiments, the applica-

tions of this invention is not limited as such. This invention can be applied to fabricate the bit lines of a memory device or some other semiconductor devices. In any case, the stress relieving method of this invention can be applied whenever a high stress film layer is formed over a wafer.

[0035] Accordingly, by breaking up the high stress film layer (the second dielectric layer) into a sheet with discontinuous surface and height difference, this invention relieves the stress within the film layer and prevents the warping of the wafer. Thus, misalignment of photoresist pattern after a photolithographic process is avoided.

[0036] Furthermore, no additional photomask is required. Hence, there is no added complexity to the fabrication process.

[0037] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.